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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,398	07/03/2003	Hossein Amidi	034559-000002	4470
<div>Robert E. Krebs Thelen Reid & Priest LLP P.O. Box 640640 San Jose, CA 95164</div>				
<div>7590 07/29/2008</div>				
EXAMINER				
DINH, TUAN T				
ART UNIT		PAPER NUMBER		
2841				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/613,398

Applicant(s)

AMIDI ET AL.

Examiner

Tuan T. Dinh

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3, 8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon et al. (U.S. Patent 6,049,476) in view of Takemae (U.S. Patent 6,650,593).

As to claims 1 and 10, Laudon et al. discloses a memory module (102) and its method comprising:

a printed circuit board (103) having a plurality of connector pins (edge connector 108);

a plurality of different types of memory devices (SDRAM 104 for data memory, and 106 for state memory or 210 and 212 in figure 2) mounted on said printed circuit board (103); and

an electrical circuit (traces or components mounted on the PCB 103) coupling said plurality of memory devices (104, 106) to said plurality of connector pins (6) such that said plurality of connector pins (6) has multiple functionality based on a respective of each of said plurality of different types of memory devices (104, 106), see column 7.

Laudon does not specific disclose the plurality of different types of memory devices having different memory architectures.

Takemae shows a memory system as shown in figure 2 comprising a printed circuit board (PCB-10) having three different types of memory devices (SDRAM-14a (volatile memory); NOR type flash-14b; and NAND type flash 14c, non-volatile memory).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Takemae employed in the module having memory devices (104, 106) of Laudon in order to utilize in storing data.

As to claim 8, Laudon et al. discloses a computer comprising: a main board (motherboard, not shown); and a memory module (102) coupled to said main board (the motherboard), said memory module including: a printed circuit board (103) having a plurality of connector pins (108); and a plurality of different types of memory devices (104 and 106, which is a DRAM and/or DDR SDRAM mounted on said printed circuit board (103), an electrical circuitry (trace pr path) electrically coupling said plurality of memory devices to said plurality of connector pins such that said plurality of connector pins has multiple functionality based on said plurality of memory devices.

Laudon does not specific disclose the plurality of different types of memory devices having different memory architectures.

Takemae shows a memory system as shown in figure 2 comprising a printed circuit board (PCB-10) having three different types of memory devices (SDRAM-14a (volatile memory); NOR type flash-14b; and NAND type flash 14c, non-volatile memory).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Takemae employed in the module having memory devices (104, 106) of Laudon in order to utilize in storing data.

As to claim 3, Laudon discloses said plurality of connector pins (108) engages with a memory socket (see column 7), said memory socket communicating with a memory controller (216).

3. Claims 2, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon in view of Takemae as applied to claims 1 and 8 above, and further in view of Prior Art (figure 2, submitted by applicant, hereafter APA).

Regarding claims 2, 9, and 11, Laudon and Takemae disclose a first type memory that is SDRAM except for a second type memory is FCRAM.

APA teaches (figure 2) a FCRAM system (200) comprising a FCRAM (204).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of APA employed in the module of Laudon and Takemae in order to provide a high speed memory performance.

4. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laudon and Takemae, and further in view of Deneroff.

As to claims 4-7, Laudon as modified by Takemae discloses all of the limitation of the claimed invention except for said memory controller includes: a plurality controllers, each controller corresponding to an architecture of one the plurality of different types of the memory devices; an Finite State Machine (FSM) coupled to said plurality of controllers; an address multiplexor coupled to said FSM, said address multiplexor communicating with said memory socket; a control multiplexor coupled to said FSM,

said control multiplexor communicating with said memory socket; and a data multiplexor coupled to said FSM, said data multiplexor communicating with said memory socket, and further comprising: a second electrical circuit said second electrical circuit coupled to said plurality of memory devices; and a plurality of testing pins, and said plurality of connector pins (6) includes 220 pins. Deneroff discloses all that limitations (see the last Office action). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Deneroff employed in the module of Laudon and Takemae in order to provide excellent operation for the user.

Response to Arguments

5. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/
Primary Examiner, Art Unit 2841.